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9-Level Voltage Source Inverter Controlled Using Selective Harmonic Elimination

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ABSTRACT

This paper presents an efficient cascaded H-bridge inverter topology that is controlled using an optimized selective harmonic elimination pulse width modulation technique. The switching angles are obtained by solving the nonlinear transcendental equation with the aid of genetic algorithm optimization method. Unlike the usual H-bridge converter topologies that require multiple individual direct current (DC) sources and additional switching components per voltage step, the proposed topology utilizes a single DC source to supply two full-bridge modules. The modified topology employs a cascaded multi-winding transformer that has two independent primary windings and series-connected secondary side with 1:E and 1:3E turn ratios. The converter topology and switching function are proven to be reliable and efficient, as the total harmonic distortion (THD) is quite low when compared with the conventional H-bridge topology controlled by other modulation techniques. This feature makes it attractive to renewable energy systems, distributed generation, and highly sensitive equipment such as those used in medical, aerospace, and military applications. The topology is simulated using a PSIM package. Simulation results show that all the 11-level lower order odd harmonics are eliminated or suppressed in compliance with the SHE elimination theorem of (N-1).

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1. INTRODUCTION

Prior to 1975, two-level inverters were the only available topologies in the market. In 1975, however, multi-level inverters were introduced. This development started with three-level topologies, which produced a quasi-square output waveform (+E, 0, -E) [1]. A number of multi-level converter topologies are currently available, and most are drawn from the three major pioneering topologies, namely, flying capacitors (FC), neutral point (NPC) /diode clamped, and cascaded H-bridge (CHB) [2],[3]. Multi-level converter is used to bridge the gaps and limitations of conventional inverters in the areas of high-power handling capability, high input and output harmonic contents, and high voltage and current switching stress on power electronic devices, all of which cumulatively lead to poor efficiency and induce electromagnetic interference (EMI) in the system [4],[5].

The multi-level voltage source inverter is capable of providing and handling high output power, which attracts power industries. Multiple output voltage steps make the inverter capable of operating in kilo to mega volt ranges. In addition to its power handling capability, it has low electromagnetic interference (EMI) and high switching freedom. Switching freedom is utilized to address the switching stress problem on

the power electronic switches and the redundancy in fault-tolerant systems. The more voltage steps there are in an inverter output waveform, the closer they are to the sinusoidal signal and thus the lesser the harmonic contents in the output. Less harmonics in the converter improves both its efficiency and reliability when compared with the conventional two-level inverter [6]. Multi-level inverter output steps are limited by increasing the power electronic components, which translate to an increase in system cost, size, and switching complexity [1].

The positive features of multi-level inverter have broaden its range of applications, including utility-based applications; electric drives; and renewable energy, including distributed generations. The inverter is equally suitable for systems that require less electromagnetic interference, including highly sensitive medical equipment and adjustable speed drive systems [1],[7].

Harmonic elimination and suppression are vital in both input and output of nonlinear circuits, especially power electronic inverters. Depending on the inverter switching frequency (high or low), modulation techniques can be used to eliminate harmonics in the output of the inverter. The high switching modulation techniques are categorized into classic carrier-based sinusoidal pulse width modulation (PWM), multi-carrier PWM classified into phase disposition (PD) and phase opposition disposition PWM, and space vector modulation (SVM) technique. The low frequency switching is categorized into staircase modulation, stepped modulation, and selective harmonic elimination pulse width modulation (SHE-PWM) [7].

SHE-PWM, otherwise known as fundamental switching frequency method, is the technique used in this paper. It is capable of directly controlling the output voltage harmonics in an inverter. Therefore, it drastically reduces the switching losses, filter size, price, and complexity of the converter circuit [8]. These qualities give it an edge over other modulation strategies. Its major drawback is the challenge in solving the nonlinear transcendental equations, which need to be solved to determine the values of the switching angles. Owing to the nonlinearity of the equation, iterative methods such as Newton–Raphson method, mathematical resultant method using the concept of polynomials, homotopy, and other techniques are employed to solve the equations [9]. The appropriate choice of initial conditions determines the solution convergence and computational time. Therefore, the farther the initial guess is from the actual solution, the more the computing time. Moreover, the trigonometric terms in the equation result in multiple solutions. Thus, optimization technique is needed for the solution to converge at the global optima [10]. In this regard, several optimization techniques were developed and analysed as comprehensively reviewed by Jacob et al., [9].

The sole objective of this paper is to generate more output voltage steps with reduced harmonic contents in the converter output by using SHE-PWM and hybrid genetic algorithm optimization reported in [11]. Thus, it hopes to address the issue of trade up between output voltage steps and converter circuit complexity. Effort was made by Kang et al., (2003) to address the same mentioned problem. Where a new converter topology with three H-bridge modules is developed. Each module has a multi-winding transformer with 1:E, 1:E, and 1:3E turn ratios. The first H-bridge module is a PWM inverter that produces chopped output voltage to compensate for the waveform step transition of the fundamental wave. The remaining two modules involve the syntheses of the fundamental output voltage level. The topology reduces the components and produces a lesser amount of total harmonic distortion (THD) compared with those of the classical topologies. The drawbacks of this method include large system size due to low-frequency transformer, high cost, and high harmonic content at light load [12]. Output steps, address, and transformer size also increase. A modified topology similar to that mentioned above was proposed by the same author in [13]. The circuit configuration is the same as that of the previously mentioned inverter, differing only in the transformer turn ratio and switching function of the PWM inverter. The former PWM inverter is operated at fundamental frequency and thus uses low-frequency transformer with a 1:E turn ratio. In this configuration, the PWM inverter is controlled at high frequency around 20 times fundamental and 1:0.5E transformer ratio. Hence, the high frequency shrinks the transformer size of the PWM inverter. The drawback of this technique is the high switching loss caused by the high switching of the PWM inverter, a drawback that affects the power electronic switch lifespan and overall system efficiency.

In this paper, the topology employed a cascaded multi-winding transformer that has two independent primary windings and a series-connected secondary side with 1:E and 1:3E turn ratios. The transformer turn ratio enables the converter to achieve more output voltage steps close to a sinusoidal waveform without additional power electronic switches and DC source. The topology generates a stable nine-level output voltage waveform. The converter topology and switching function have been proven to be reliable and efficient, as the THD is quite low when compared with the conventional H-bridge topology controlled by other modulation techniques. The variation efficiency and THD based on output load in both two cases are evaluated. The proposed configuration has less THD and better efficiency compared with the conventional configuration due to its capability to selectively eliminate the lower odd order lower harmonics. The remaining high-order harmonics are eliminated using a small-sized high frequency filter or mitigated by the transformer magnetizing inductance.

2. MATERIALS AND METHODS

2.1. Converter Circuit Configuration and Operation

Figure 1 depicts the circuit configuration of the converter topology used in this research. The converter consists of two parallel connected H-bridge modules fed through a single DC supply. The source can be Photovoltaic, Wind, lithium-ion battery or even fuel cell. Each of the modules has four semiconductor switches and is conFig.d such that it can generate a quasi-square voltage waveform (+E, 0, –E) at its output terminal. E is assumed to be the input DC value from the power supply unit. S1, S2,...S8 are the semiconductor gating signals. Term1, Term2, Term3 and Term4 are the output terminals of the respective bridges. The terminal pairs are connected to the primary winding of a specially designed multi-winding transformer that has series-connected secondary. Given the proper switching sequence of the power electronic switches coupled with appropriate transformer turn ratio, a nine-level output waveform is generated at the transformer series-connected secondary. This converter topology has an additional advantage of a higher number of switching redundancy states that can be utilized to generate different voltage steps with the same circuit configuration and employed in fault-tolerant systems. SHE-PWM is the modulation technique used to generate the output waveform. The power switches are controlled such that the lower order odd harmonics are eliminated, living behind the even harmonics, which are expected to be canceled out based on quarter-wave symmetry theorem.

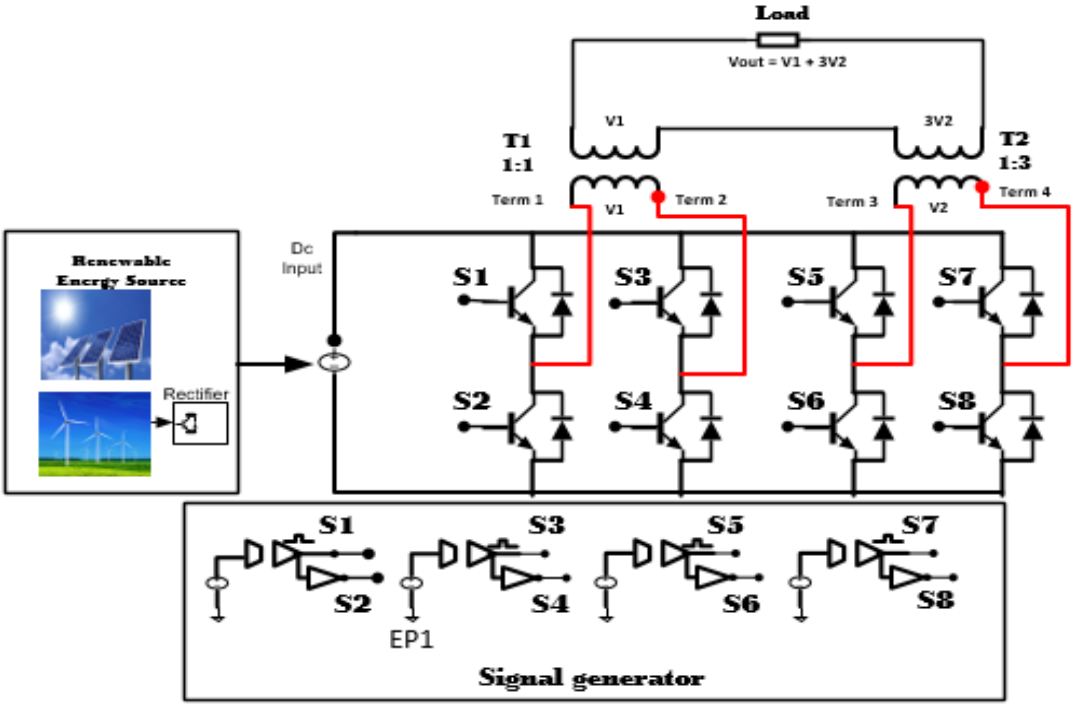


Figure 1. Proposed converter topology

2.2. Fundamental Voltage Waveform Design and Switching Angle Computations

As mentioned earlier, the proposed circuit topology is capable of generating different output voltage waveforms using the redundant switching states. However, this paper is only interested in investigating nine-level output waveform with normalized fundamental component M=3.2 and switching angle distribution ratio of 3/3/3/3.

The modulation employed on any kind of converter topology plays a major role in determining the properties of its output waveform [14]. As stated earlier, selective harmonic elimination is the modulation technique to be used for generating the nine-level output voltage. To achieve this, the switching angles must be carefully selected such that the lower order odd harmonics are eliminated. This technique, apart from producing an output with a lower THD, also reduces the amount of electro-magnetic interference and switching losses caused by high switching frequency modulation techniques [15],[16].

To have an idea on how the angle distribution ratio should be (3/3/3/3), a rough sketch of the nine-level waveform was initially made using an arbitrary values of switching angles. Figure 2 depicts a rough

sketch of the targeted nine-level waveform with the assumption that it obeys the quarter-wave symmetry theorem; that is, it has 12 switching angles (α1 to α12) per quarter cycle [17].

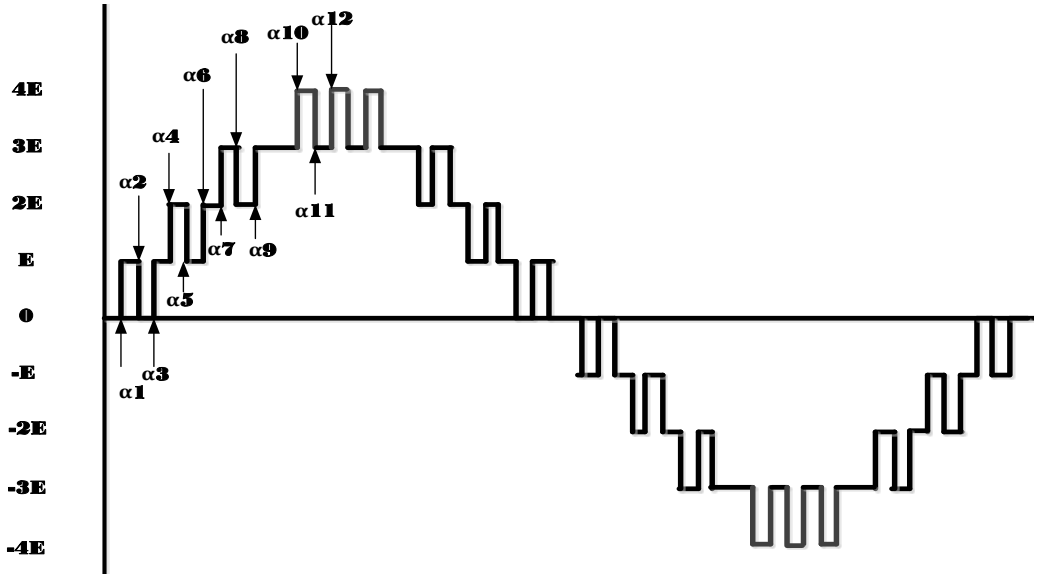


Figure 2. Nine Levels waveform with 3/3/3/3 distribution ratio.

Based on the quarter theorem, a single-phase sinusoidal wave causes the DC and even harmonic components to cancel out, and only the fundamental and odd harmonic components remain [18]. To eliminate the odd harmonics, the fundamental component needs to be systemically controlled during both the positive and negative half cycles at certain specified angles. With this operation, the selected lower order odd harmonics (N-1) are eliminated (Where N is the number of switching angles) [17,19]. Therefore, 3rd, 5th, 7th, 9th, 11th, 13th, 15th, 17th, 19th, 21st and 23rd order harmonics are all eliminated in this case.

Based on the quarter-wave symmetry, the Fourier series expansion of the nine-level waveform in Figure. 2 is given by the below expression [20].

$$V_{out}(wt) = \sum_{n=1}^{\infty} a_n \ \sin(nwt) \tag{1}$$

Where

$$a_n = \frac{4E}{n\pi} \sum_{K=1}^{N} (-1)^{K+1} \cos(n\alpha_K) \tag{2}$$

for odd values of n

$$b_n = 0 \tag{3}$$

for all value of n

α_K Denotes the switching angles and most satisfies the relationship, (4)

$\alpha_1 < \alpha_2 < \ldots\ldots < \alpha_N < \frac{\pi}{2}$

Simplifying Equation 1 and 2 The amplitude of the fundamental and non-triplen odd harmonic components in the five-level output waveform is represented by the non-linear transcendental equations given in Equation.5 and 6:

$$h_1 = \frac{4*E}{\pi}\{\cos(\alpha_1) - \cos(\alpha_2) + \ldots\ldots \pm \cos(\alpha_{12})\} \tag{5}$$

$$h_1 = \frac{4*E}{n\pi}\{\cos(n\alpha_1) - \cos(n\alpha_2) + \ldots \pm \cos(n\alpha_{12})\} \tag{6}$$

The amplitude of the fundamental component is controlled by the modulation index (M) and is given by the expression.

$$\text{Modulation Index (M)} = \frac{h_1}{E} \quad (7)$$

For all n = 1 While M=0 for all n + 1

Hence, using Equation (5), (6) and (7) the non-linear transcendental equations can be expressed as:

$$\cos(\alpha_1) - \cos(\alpha_2) + \cos(\alpha_3) - + \cos(\alpha_{11}) - \cos(\alpha_{12}) = \frac{M\pi}{4} \quad (8)$$

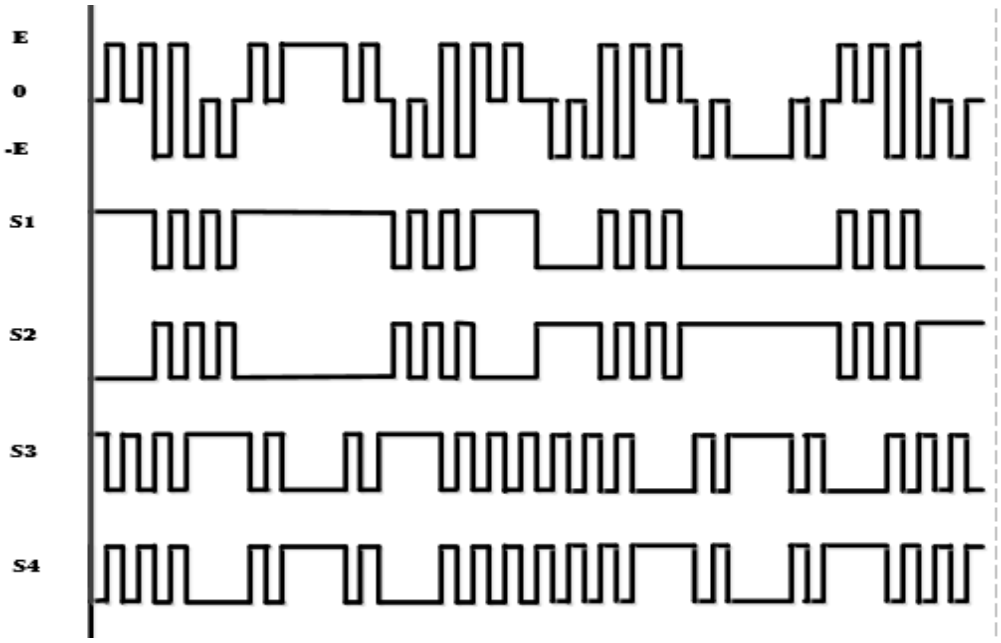
$$\cos(3\alpha_1) - \cos(3\alpha_2) + \cos(3\alpha_3) - .. + \cos(3\alpha_{11}) - \cos(3\alpha_{12}) = 0 \quad (9)$$

$$\cos(23\alpha_1) - \cos(23\alpha_2) + \cos(23\alpha_3) - .. + \cos(23\alpha_{11}) - \cos(23\alpha_{12}) = 0 \quad (10)$$

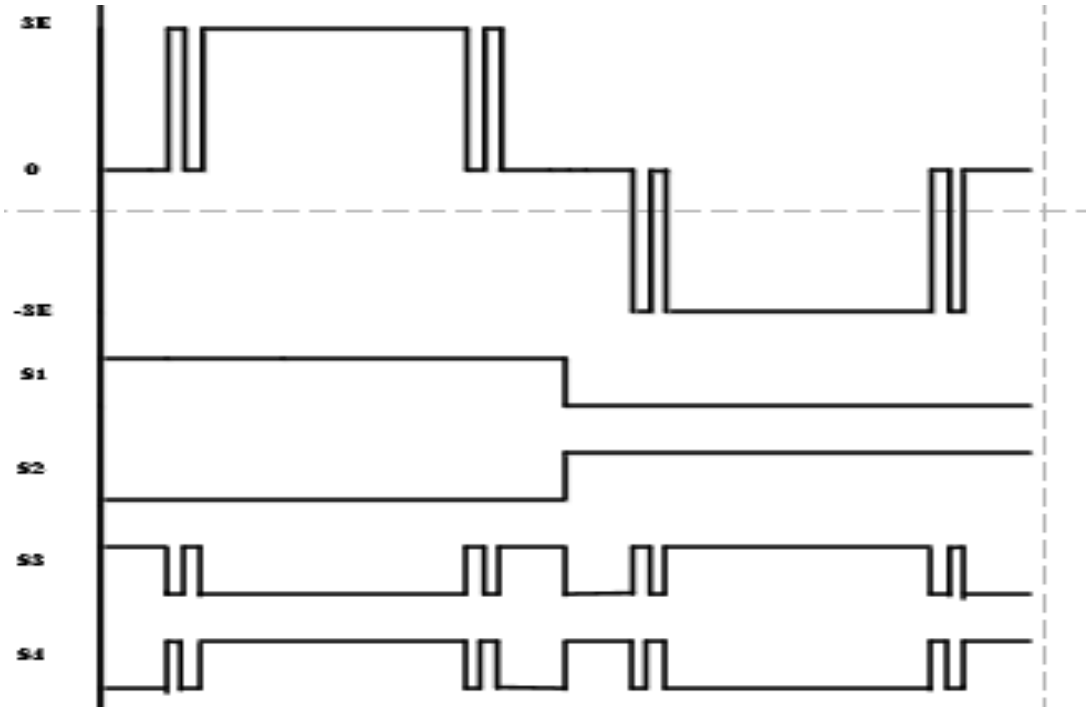
The above nonlinear transcendental equations are solved to find the approximate close value of the switching angles, which are capable of eliminating the output lower order harmonics. Given the nonlinearity of the equations, finding the solution using ordinary mathematical solution methods is not possible. Therefore, the hybrid genetic algorithms presented in [11] was used to find the solution for the 12 switching angles. The technique uses different values of over modulation index (M) to find the solutions for the switching angles $\alpha_1, \alpha_2, \ldots, \alpha_{12}$.

2.3. Module Terminal Voltage Design and Gating Signals Generation

Figure 3a and 3b shows the targeted output voltage waveforms at the terminals of module 1 and 2 with their respective gating signals. The generated voltages were then passed through the customized multi-winding transformer. that synthesizes and compensate for the step level, whereas the second module generates the fundamental output voltage. A nine-level waveform is generated at the secondary similar to the one shown in Figure. 2. To generate the voltage waveform, the gating signal of each IGBT needs to be generated based on the calculated switching angles.



(a)



(b)

Figure 3. Designed converter terminal voltages
(a) H-bridge Module 1 terminal voltage (V1) and gating signals.
(b) H-bridge Module 2 terminal voltage (V2) and gating signals.

Majority of the notches comes from the first module that synthesizes and compensate for the step level, whereas the second module generates the fundamental output voltage. A nine-level waveform is generated at the secondary similar to the one shown in Figure. 2. To generate the voltage waveform, the gating signal of each IGBT needs to be generated based on the calculated switching angles. The IGBT's conduction states during the positive and negative half cycle in both H-bridges are given in Table 1, note other redundant switching states can as well be explored in order to address switching stress and failure of the switches. It is worth mentioning that switches on the same leg are operated complementarily to avoid short-circuiting the dc source.

Table 1 Selected switching combinations

Voltage	Switching states							
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
0	1	0	1	0	1	0	1	0
+E	1	0	0	1	1	0	0	1
0	0	1	0	1	0	1	0	1
-E	0	1	1	0	0	1	1	0

3. RESULTS AND DISCUSSION

3.1. Switching Angles Solutions

To assess the performance of the proposed nine-level multi-level voltage source inverter, the design procedures and proposed circuit topology were implemented using a PSIM software package. The circuit was simulated using the calculated switching angles with modulation index M= 3.2 and distribution ratio of 3/3/3/3, which means 12 switching points, were present per quarter cycle. Based on selective harmonic elimination theory, the converter eliminated (N-1) harmonics, which means that all the 11 lower order odd harmonics(3^{rd}, 5^{th}, 7^{th}, 9^{th}, 11^{th}, 13^{th}, 15^{th}, 17^{th}, 19^{th}, 21^{st}, 23^{rd}) were either eliminated or suppressed [18],[19]. Table 2 shows the 12 calculated values of the switching angles in degrees and the equivalent time values in milliseconds (ms). The remaining angles were calculated based on quarter wave symmetry theory.

Table 2 Nine level Voltage level 3/3/3/3 M_I= 3.2

S/N	0-90	90-180	180-270	270-360
1	5.9272	174.0728	185.9272	354.0728
2	9.3878	170.6122	189.3878	350.6122
3	12.3888	167.6112	192.3888	347.6112
4	22.1571	157.8429	202.1571	337.8429
5	24.6285	155.3715	204.6285	335.3715
6	29.2705	150.7295	209.2705	330.7295
7	45.9568	134.0432	225.9568	314.0432
8	51.0958	128.9042	231.0958	308.9042

3.2. Topologies Device Counts Comparison

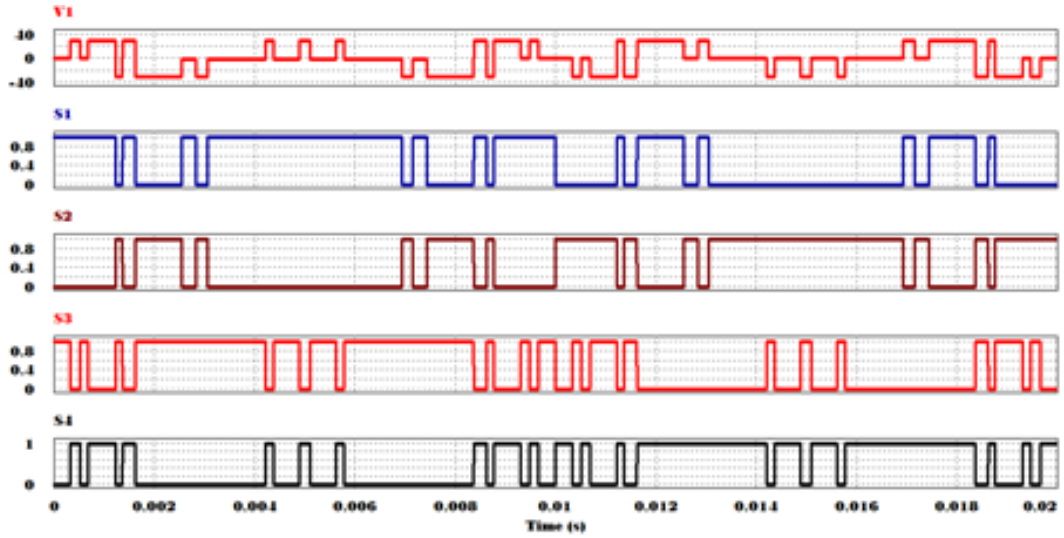
Table 3 presents the component comparison between the conventional nine-level multi-level inverter topologies comprising the diode clamp, flying capacitor, cascaded H-bridge, and the proposed modified nine-level topology. As seen from the table, all the topology number of components doubled that of the proposed. For instance, the number of clamping diodes in the diode clamp topology increased with rising voltage level. This condition brought about additional cost and circuit complexity, especially in higher output voltage steps. It also suffered a drawback due to the unequal switching stress across the power electronic switches (i.e., inner switches conduct for a longer duration compared with the outer switches). Its non-modular nature makes it unsuitable for redundancy application [8],[21],[22]. In the case of the flying capacitor topology, the number of voltage-balancing capacitors increased with increasing output steps. The capacitors also required a complex feedback circuitry to maintain their voltage level, which makes the overall circuit bulky and difficult to package [23],[24]. For the cascaded H-bridge, the need for individual DC input source and isolation transformers are regarded as its major drawbacks, even though it has relatively less device count compared with the previously mentioned topologies [13],[21],[25]. Hence, our modified nine-level cascaded H-bridge topology has less device count, size, and cost compared with the equivalent nine-level topologies of the conventional converter.

Table 3. Components Comparison Between Conventional 9-Level Multi-Leve Inverter Topologies And The Proposed

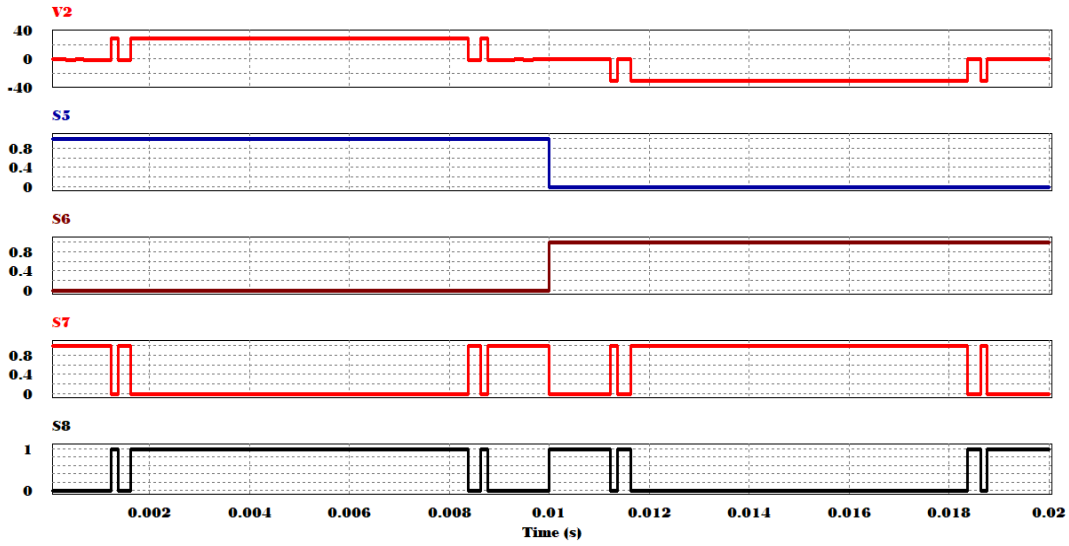
Topology Type	No of switches	Gate Drivers	Clamping Diode	Balancing Capacitor	Dc-Bus	Transformer
Diode-Clamp (DC)	2*(K-1) =16	16	(K-1)(K-2) 56	Nil	(K-1) =8	Nil
Flying Capacitor (FC)	2*(K-1) =16	16	Nil	(K-1)(K-2)/2 =28	(K-1) =8	Nil
Cascaded H-Bridge (CHB)	2*(K-1) =16	16	Nil	Nil	(K-1)/2 =4	4
Proposed Topology	4*H =8	8	Nil	Nil	1	1

3.3. Simulation Results

The proposed topology modular terminal voltage waveforms V1 and V2, together with their corresponding control signals of IGBT, are shown in Figure. 4a and 4b, respectively. Both voltage waveforms look the same with the pre-sketch pattern presented in the previous section. The gating signals for the eight IGBT's are switched in conformity with the voltage switching combination presented in Table 1.



(a)



(b)

Figure. 4 Simulated Converter Terminal Voltage
(a) Simulated output terminal voltage for bridge module1 (V1) with gating signal.
(b) Simulated output terminal voltage for bridge module2 (V2) with gating signal.

Figure 5a shows the nine-level fundamental output voltage waveform across a resistive load. The fundamental voltage was chopped several times at pre-calculated switching points, which satisfies the 3/3/3/3 distribution ratio as sketched in Figure. 2. Note that the output voltage across the resistive load is expressed as the sum of both transformer secondary side voltages ($V_{0ut} = V_1 + 3V_2$), as shown in Figure. 5b.

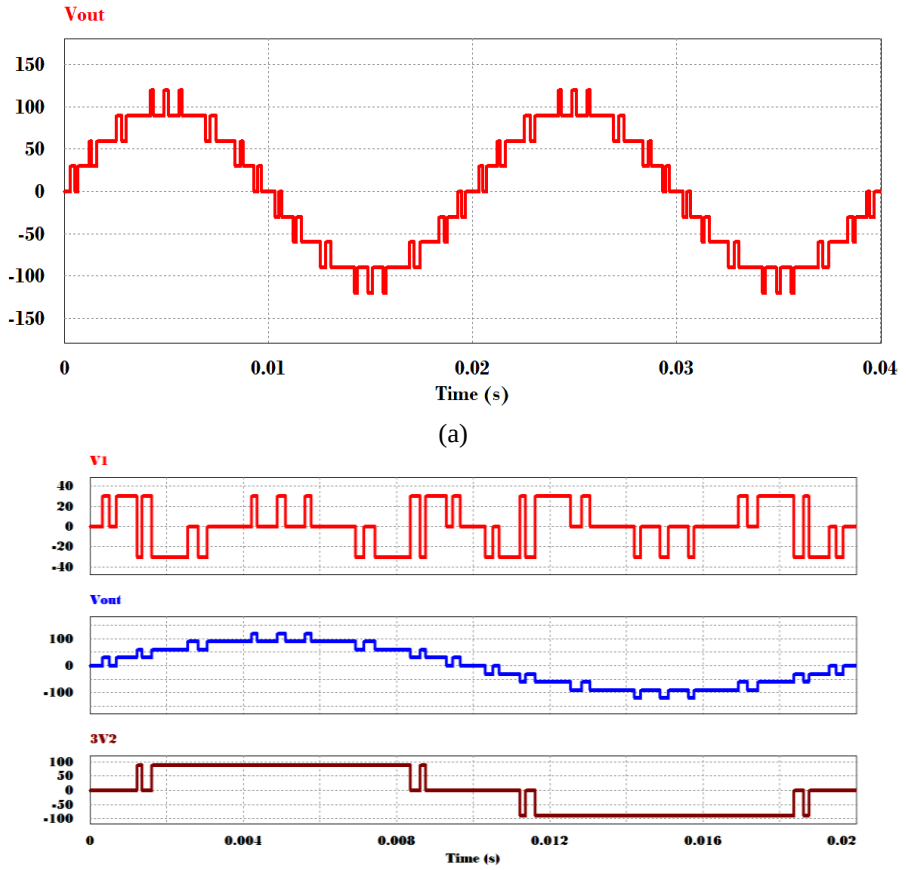
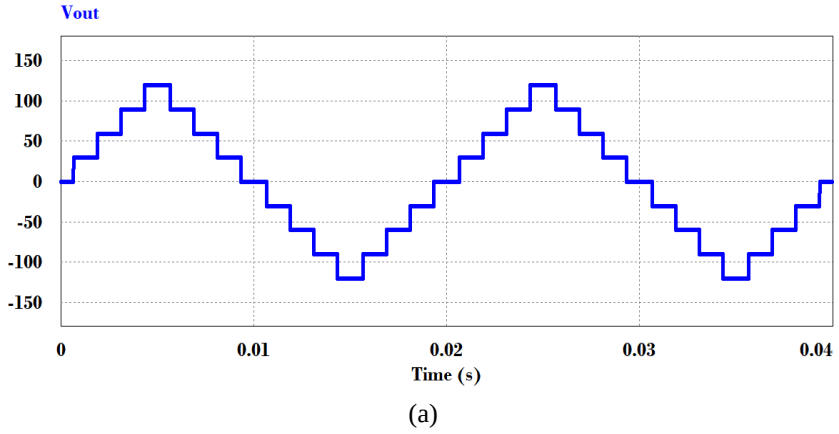
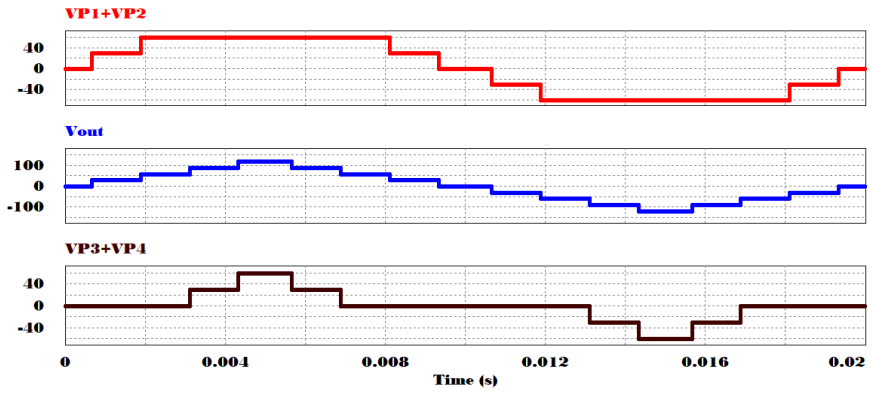


Figure. 5 (a) The proposed Nine-level waveform. (b) The terminal voltages V_1, Vout and $3V_2$

To illustrate the difference between the proposed topology waveform and the classical cascaded H-bridge, a nine level circuit was also simulated, and the waveform is shown in Figure. 6a. As outlined in Table 2, it has four separate modules, each having an independent DC source and an output transformer with 1:1 turn ratio. For the image quality, the terminal voltages are shown as the sum of the first two modules $Vp_1 + Vp_2$ and the last two $Vp_3 + Vp_4$ voltages in Figure. 6b. All these add up to produce a nine-level output waveform.

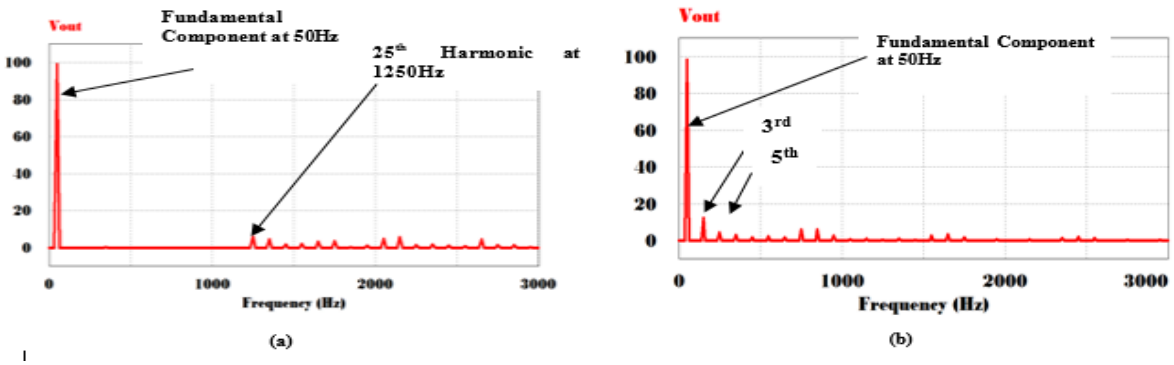




(b)

Figure. 6 (a) Classical Nine-level waveform (b) Terminal voltages VP1+VP2, Vout and VP3+VP4

Figure 7a shows the fast Fourier transform (FFT) of our proposed nine-level over the range of 3 KHz. From the spectrum, SHE-PWM successfully eliminates all the 11 selected lower order harmonics that lies within a 1.15 KHz (23rd) range. The first dominant harmonic appears at 1.25 KHz, which is the 25th harmonic. Based on the sequence, it is the 12th lower order odd harmonic, which falls outside the (N-1) range. This graph further validates the effectiveness of our proposed converter. Figure. 7b is the FFT of the nine-level cascaded H-bridge topology. Clearly, the lower order odd harmonics (3rd, 5th....etc) are only suppressed not eliminated, unlike in the case of our proposed topology.



(a) (b)

Figure. 7 FFT Spectrum of a nine-voltage source converter.
(a) FFT for Modified CHB topology. (b) FFT for Conventional CHB topology.

Figures 8a and 8b show the relationship between the total harmonic distortions considered over the 100th harmonics and the output power of the two nine-level converter topologies. From the plot, the THDs of both converters decrease with increasing output power, especially in the proposed case by looking at its sharp negative gradient. From the Figure. 8a, the THDs of both converters at 1 kW stand at 14.64% and 18.11%, respectively. These values are above the required IEEE 5% standard, because the SHE techniques target only the first 11 lower odd harmonics. To meet the required standard, a filter capable of filtering the 25th harmonic needs to be connected. Figure b shows the THD value after filtering the 25th harmonic upward for both cases. The proposed topology performs excellently because the THD at 1 kW stands at approximately 0.425%, which satisfies the IEEE standard. Meanwhile, as expected, the conventional topology falls slightly below its former value to 16.81%. Its THD is still high because the lower order harmonics are the major contributors to THD due to their high amplitude, as can be seen from the FFT spectrum.

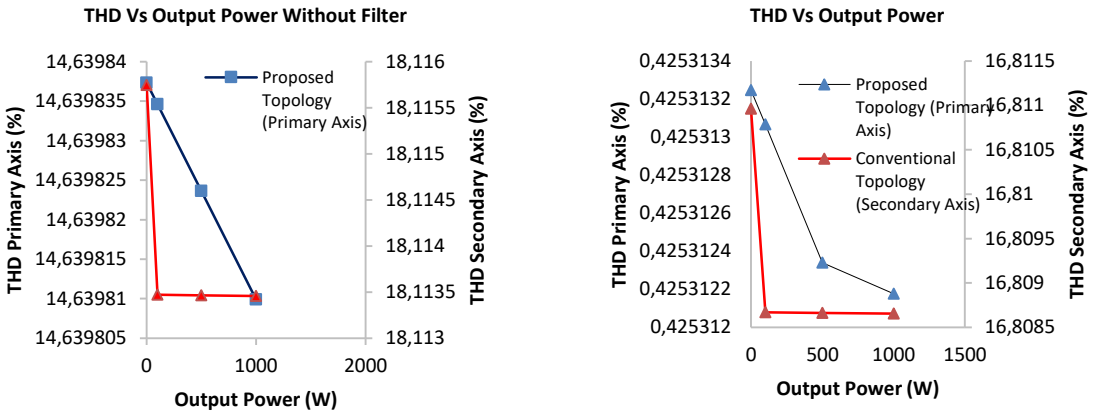


Figure. 8 THD Comparison.
(a) Without output Filter (b) With output Filter

Figure 9 shows the efficiency comparison plot of the two converters. Both converters dissipate similar behaviors. At minimum or no-load both converters have very poor efficiency. However, efficiency improves and reaches a steady state when the load increases. The average efficiency values for the proposed and conventional topologies are 72% and 80%, respectively. This finding concludes that the proposed topology has better operational efficiency than the conventional one.

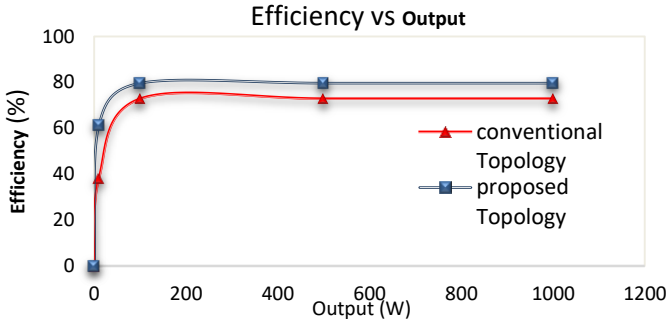


Figure. 9 Efficiency comparison

4. CONCLUSION

A nine-level multilevel converter using cascaded H-bridge topology with a single DC input source and multi-winding transformer was designed and simulated. The reported converter addressed the issue of using multiple independent DC-link sources to synthesize nine-level output voltage waveforms and reduce the number of transformers compared with that of ordinary conventional multi-level converters generating the same number of voltage levels. It can be deduced that SHE-PWM has the capability of eliminating selected harmonics by adding a number of notches to the fundamental component at a specific pre-determined angle. It also satisfies the IEEE standard of less than 5% THD. The converter is compact in size, less complex, and has a lower cost of production and maintenance. These advantages make the converter suitable for electric vehicles and distributed generation applications.

The theoretical and simulation results were verified. All the results obtained yielded positive outcomes, which provided the converter an advantage over its counterparts and the possibility of taking the lead in both automotive and renewable energy applications.

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